EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1246	(store near3 (queue buffer FIFO)) same enable same (byte bit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:51
S2	148	(store near3 (queue buffer FIFO)) same enable same (byte bit) same updat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:51
S3	167	(store near3 (queue buffer FIFO)) same enabl$4 same (byte bit) same updat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:52
S4	28	S3 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:59
S5	489	dispatch$4 with (store near3 (queue buffer FIFO))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:59
S6	100	S5 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:59
S7	70	dispatch$4 with (store near3 (queue buffer FIFO)) with full	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 10:59
S8	16	S7 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:02

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S9	168	updat$4 with (store near3 (queue buffer FIFO)) with entry	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:03
S10	61	S9 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:10
S11	71	updat$4 with cache with (address near2 only)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:12
S12	4	updat$4 with cache with (address near2 only) with (full entire)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:12
S13	184	updat$4 with cache with (data) with (full entire)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 16:53
S14	250	byte adj enable adj bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:17
S15	121	(byte adj enable adj bit) and (cache near3 line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:18
S16	42	(byte adj enable adj bit) and (cache near3 line) and updat$4 with (store near2 (queue buffer))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:23

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S17	1	(byte adj enable adj bit) and (cache near3 line) and (updat$4 with (store near2 (queue buffer)) with full)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:24
S18	39	(byte adj enable adj bit) and (cache near3 line) and ((store near2 (queue buffer)) with full)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:25
S19	39	(byte adj enable adj bit) and ((store near2 (queue buffer)) with full)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:25
S20	66	(byte near2 enable near2 bit) and ((store near2 (queue buffer)) with full)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/13 11:25
S21	184	full same updat$4 same current same cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 16:55
S22	0	(granule with full) same updat$4 same current same cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 16:55
S23	1	(granule with full) same updat$4 same cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 16:55
S24	1	granule same full same updat$4 same cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 16:58

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S25	42	cache and (granule same full)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:01
S26	1150	cache with updat$4 with without	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:01
S27	130	cache with updat$4 with without with copy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:02
S28	99	S27 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:01
S29	1	cache with updat$4 with without with current with copy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:02
S30	22	cache with updat$4 with without with current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:04
S31	45	(RC (read near3 claim)) and granule and cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:08
S32	24	S31 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:13

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S33	6	("5404550" | "5894569" | "5940611" | "5956503" | "6101568" | "6247114").PN. OR ("7089364"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/09/27 17:05
S34	470	(RC (read near3 claim)) and (store near3 (queue buffer FIFO)) and cache	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:08
S35	21	(RC (read near3 claim)) and (store near3 (queue buffer FIFO)) and cache and granule	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:09
S36	378	(RC (read near3 claim)) and (store near3 (queue buffer FIFO)) and dispatch$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:09
S37	9	(RC (read near3 claim)) same (store near3 (queue buffer FIFO)) same dispatch$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:12
S38	491	(store near3 (queue buffer FIFO)) with dispatch$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:13
S39	80	((store near3 (queue buffer FIFO)) with dispatch$4) same full	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:13
S40	18	S39 and "711".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/09/27 17:17
S41	3899	(711/118,122,133,141 710/310).ccls.	USPAT	OR	ON	2007/09/27 17:39

EAST Search History Interference Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1621	(711/118,122,133,141 710/310).ccls.	US-PGPUB	OR	ON	2007/09/27 18:22
L2	2	(store near2 queue near2 mechanism).clm. and L1	US-PGPUB	OR	ON	2007/09/27 18:23
L3	1	(RC near2 mechanism).clm. and L1	US-PGPUB	OR	ON	2007/09/27 18:23
L4	1	(storage adj granule).clm. and L1	US-PGPUB	OR	ON	2007/09/27 18:23
L5	2	(address-only adj operation).clm. and L1	US-PGPUB	OR	ON	2007/09/27 18:34
L6	1	(cache adj update adj mechanism).clm. and L1	US-PGPUB	OR	ON	2007/09/27 18:34

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Result # 1 Relevance: ○○○○○

Simulation of Telecommunication Line Equipment

1971-07-01 IPCOM000075041D English (United States)

Telecommunication terminals and line equipment may be simulated on an IBM System/360 which has been designed to operate as a terminal message interchange (TI). There are two parts to the simulation: 1) Line buffers and line buffer controls which simulate the ...

Result # 2 Relevance: ○○○○

Image System Quality and Data Compression Enhancement by Excision of Isolated Single Pels and Quad Pel Groups

1989-02-01 IPCOM000034384D English (United States)

In image data systems, halftone patterns and other high amplitude noise severely impact data compression and reduce image quality. Excision of isolated (unconnected) pels and quads of pels effects significant image quality and data compression enhancement. (Image Omitted) ...

Result # 3 Relevance: ○○

Method for dynamic lockout avoidance in a SMT processor

2005-01-04 IPCOM000033913D English (United States)

In a simultaneous multi-threaded (SMT) processor, a thread may become "locked out" if it is blocked from making forward progress by the other thread(s). Disclosed is a method to dynamically avoid thread "lockout" by guaranteeing that each thread make ...

Result # 4 Relevance: ○○

Receive buffer optimization

2006-06-26 IPCOM000137633D English (United States)

Today, a consumer (e.g. application layer middleware) utilizing Remote Direct Memory Access (RDMA) verbs in compliance with the InfiniBand (IB) or Internet Wide Area RDMA Protocol (iWarp) specifications will create a Memory Region (MR) or Memory Window (MW) on the host. The ...

Result # 5 Relevance: ○○

Multi Byte Dataflow Techniques with Single Byte Controls

1994-04-01 IPCOM000111871D English (United States)

This invention is a series of techniques for improving performance on a DASD (Direct Access Storage Device) control unit. They involve speeding up a single-byte-wide data path by widening it to several bytes wide. However, both the architecture and the existing microcode, ...

Result # 6 Relevance:

Store Purge Pipeline for Mid-Range Processor

1990-09-01 IPCOM000101903D English (United States)

A design and implementation of a multiprocessor system requires overcoming a significant number of design and implementation hurdles. This article deals with the problems encountered in keeping caches coherent. It guarantees all system caches stay coherent and in all ...

Result # 7 Relevance:

INFORMATION FLOW IN PARALLEL PROGRAMS: AN AXIOMATIC APPROACH

1899-12-30 IPCOM000148254D English (United States)

v INFORMATION FLOW IN PARALLEL PROGFUd.IS: AN AXIOMATIC A:PPROACN by Richard Philip Reitman TR 78-350 a. i). diS ~~~;t4~~h, ," parhiu 04 IT#vu*, i"~ -b L Y r i 0 ,$Fh84? This research was supported by National Science Foundation .G grant ...

Result # 8 Relevance:

ARCHITECTURE OF AN EXPERIMENTAL OFFICE SYSTEM: The Soft Display Word Processor

1978-12-01 IPCOM000131356D English (United States)

The SDWP system is designed for use by secretarial and clerical personnel to fill in forms, create and edit the texts of documents, and store and retrieve documents electronically. The basic I/O devices include a typewriter-style (capacitanceswitch) keyboard, a CRT display, ...

Result # 9 Relevance:

Address Stream Capture

1976-08-01 IPCOM000086318D English (United States)

This scheme permits the capture of address streams with a minimum storage requirement. In order to analyze the performance effects of various design alternatives in the memory hierarchy area, it is desirable to be able to capture address streams from a running computer ...

Result # 10 Relevance:

SPECIAL FEATURE: Component Progress: Its Effect on High- Speed Computer Architecture and Machine Organization

1978-04-01 IPCOM000131297D English (United States)

Anyone concerned with understanding the past, present, and future of high-speed computing must of necessity focus on progress in the components field. He must formulate searching questions about

the outlook of that technology and how it affects progress in high-speed ...

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Result # 11 Relevance:

Switch for a Buffer Reduction in a Multiple Transponder System

1983-01-01 IPCOM000044902D English (United States)

A multitransponder satellite communications controller is disclosed, which minimizes the buffer requirements for the receive buffers.

Result # 12 Relevance:

Method and apparatus to allow execution of Multi Row SQLs over DRDA and a) without modifying SQLs in existing application programs b) for Database clients with low Virtual Storage.

2006-09-25 IPCOM000140882D English (United States)

Disclosed below is a Method and apparatus to allow execution of Multi Row SQLs over DRDA and a) without modifying SQLs in existing application programs b) for Database clients with low Virtual Storage. The DRDA (Distributed Relational Data Architecture) protocol used ...

Result # 13 Relevance:

A DISTRIBUTED DATA AND CONTROL DRIVEN MACHINE: PROGRAMMING AND ARCHITECTURE

1978-11-30 IPCOM000150890D English (United States)

W. Ruggiero Computer Science Department School of Engineering and Applied Science University of California Los Angeles, California 90024 Pu bl ished November 1978 Prepared for the U.S. Department of Energy (formerly U . S. Energy Research and Development ...

Result # 14 Relevance:

Method to Provide Reading Synchronization Between Redundant Processors with Conflicting Measurements

2007-04-05 IPCOM000149692D English (United States)

This invention is a method to provide reading synchronization for redundant processors in a system which potentially could have conflicting values for common items each processor is reading. Using this solution will enable synchronized values to be maintained in the system ...

Result # 15 Relevance:

UNIVERSITY OF MICHIGAN Memorandum 27 MOMS: MICHIGAN'S OWN MATHEMATICAL SYSTEM

1970-04-01 IPCOM000128392D English (United States)

This report describes an interactive mathematical system with graphical input and output capabilities. The system was programmed during the winter of 1968 by the members of the advanced systems programming course, Computer and Communication Sciences 673, under the direction ...

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Result # 1 Relevance:

Storage Access Mechanism for Vector Operands

1994-12-01 IPCOM000114497D English

Disclosed is an invention which improves the performance of vector operations in a mul environment by basing an operand's storage access on the operation's stride.

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